IN THE CLAIMS:

1.-28. (Cancelled)

29. (New) A storage device, comprising:

a system interface unit which carries out interface with a host system via an

external bus;

a controller coupled with said system interface which analyzes commands

received by said system interface unit from said host system and controls operations

to be performed within said storage device; and

a non-volatile semiconductor memory coupled with said controller,

wherein said non-volatile semiconductor memory is electrically erasable and

electrically programmable and stores data from said host system via said system

interface unit, and

wherein, in response to a read command received by said system interface

unit, said controller carries out concurrent operations of data transferring of data after

data processing to said host system via said system interface unit and of data

transferring of subsequent data for data processing from said non-volatile

semiconductor memory to said controller.

30. (New) A storage device as claimed in Claim 29, wherein said concurrent

operations of said data transferring of data after said data processing to said host

system via said system interface unit and of data transferring of subsequent data for

said data processing from said non-volatile semiconductor memory are carried out by two memories and by said controller.

31. (New) A storage device as claimed in Claim 30, wherein, in response to said read command received by said system interface unit, one of said two memories originates said data after said data processing and another of said two memories originates said subsequent data for said data processing.

32. (New) A storage device as claimed in Claim 30, wherein said one and said other of said two memories are said non-volatile semiconductor memory.

33. (New) A storage device as claimed in Claim 32, wherein said non-volatile semiconductor memory is a flash memory.

34. (New) A storage device as claimed in Claim 31, wherein said one and said other of said two memories are said non-volatile semiconductor memory.

35. (New) A storage device as claimed in Claim 34, wherein said non-volatile semiconductor memory is a flash memory.

36. (New) A storage device as claimed in Claim 32,

wherein said one of said two memories is coupled with said controller via a first memory bus, and said other of said two memories is coupled with said controller via a second memory bus,

wherein, during said data transfer of said data after said data processing, said data after said data processing is transferred to said host system via said system interface and said subsequent data for said data processing is transferred from said other of said two memories to said controller via said second memory bus, and

wherein, during said data transfer of said subsequent data after said data processing, said subsequent data after said data processing is transferred to said host system via said system interface and further subsequent data for said data processing is transferred from said one of said two memories to said controller via said first memory bus.

37. (New) A storage device as claimed in Claim 33,

wherein said one of said two memories is coupled with said controller via a first memory bus, and said other of said two memories is coupled with said controller via a second memory bus,

wherein, during said data transfer of said data after said data processing, said data after said data processing is transferred to said host system via said system interface and said subsequent data for said data processing is transferred from said other of said two memories to said controller via said second memory bus, and

wherein, during said data transfer of said subsequent data after said data processing, said subsequent data after said data processing is transferred to said host system via said system interface and further subsequent data for said data processing is transferred from said one of said two memories to said controller via said first memory bus.

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38. (New) A storage device as claimed in Claim 34,

wherein said one of said two memories is coupled with said controller via a first memory bus, and said other of said two memories is coupled with said controller via a second memory bus,

wherein, during said data transfer of said data after said data processing, said data after said data processing is transferred to said host system via said system interface and said subsequent data for said data processing is transferred from said other of said two memories to said controller via said second memory bus, and

wherein, during said data transfer of said subsequent data after said data processing, said subsequent data after said data processing is transferred to said host system via said system interface and further subsequent data for said data processing is transferred from said one of said two memories to said controller via said first memory bus.

39. (New) A storage device as claimed in Claim 35,

wherein said one of said two memories is coupled with said controller via a first memory bus, and said other of said two memories is coupled with said controller via a second memory bus,

wherein, during said data transfer of said data after said data processing, said data after said data processing is transferred to said host system via said system interface and said subsequent data for said data processing is transferred from said other of said two memories to said controller via said second memory bus, and

wherein, during said data transfer of said subsequent data after said data processing, said subsequent data after said data processing is transferred to said

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host system via said system interface and further subsequent data for said data

processing is transferred from said one of said two memories to said controller via

said first memory bus.

40. A storage device, comprising:

a system interface unit which carries out interface with a host system via an

external bus;

a controller coupled with said system interface which analyzes commands

received by said system interface unit from said host system and controls operations

to be performed within said storage device; and

a non-volatile semiconductor memory coupled with said controller,

wherein said non-volatile semiconductor memory is electrically erasable and

electrically programmable and stores data from said host system via said system

interface unit, and

wherein, in response to a read command received by said system interface

unit, said controller carries out parallel operations of data transferring of data after

data processing to said host system via said system interface unit and of data

transferring of subsequent data for data processing from said non-volatile

semiconductor memory.

41. (New) A storage device as claimed in Claim 40, wherein said parallel

operations of said data transferring of data after said data processing to said host

system via said system interface unit and of data transferring of subsequent data for

said data processing from said non-volatile semiconductor memory are carried out by two memories and by said controller.

42. (New) A storage device as claimed in Claim 41, wherein in response to said read command received by said system interface unit, one of said two memories originates said data after said data processing and another of said two memories originates said subsequent data for said data processing.

43. (New) A storage device as claimed in Claim 41, wherein said one and said other of said two memories are said non-volatile semiconductor memory.

44. (New) A storage device as claimed in Claim 43, wherein said non-volatile semiconductor memory is a flash memory.

45. (New) A storage device as claimed in Claim 42, wherein said one and said other of said two memories are said non-volatile semiconductor memory.

46. (New) A storage device as claimed in Claim 45, wherein said non-volatile semiconductor memory is a flash memory.

47. (New) A storage device as claimed in Claim 43,

wherein said one of said two memories is coupled with said controller via a first memory bus, and said other of said two memories is coupled with said controller via a second memory bus,

wherein, during said data transfer of said data after said data processing, said

data after said data processing is transferred to said host system via said system

interface and said subsequent data for said data processing is transferred from said

other of said two memories to said controller via said second memory bus, and

wherein, during said data transfer of said subsequent data after said data

processing, said subsequent data after said data processing is transferred to said

host system via said system interface and further subsequent data for said data

processing is transferred from said one of said two memories to said controller via

said first memory bus.

48. (New) A storage device as claimed in Claim 44,

wherein said one of said two memories is coupled with said controller via a

first memory bus, and said other of said two memories is coupled with said controller

via a second memory bus,

wherein, during said data transfer of said data after said data processing, said

data after said data processing is transferred to said host system via said system

interface and said subsequent data for said data processing is transferred from said

other of said two memories to said controller via said second memory bus, and

wherein, during said data transfer of said subsequent data after said data

processing, said subsequent data after said data processing is transferred to said

host system via said system interface and further subsequent data for said data

processing is transferred from said one of said two memories to said controller via

said first memory bus.

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49. (New) A storage device as claimed in Claim 45,

wherein said one of said two memories is coupled with said controller via a first memory bus, and said other of said two memories is coupled with said controller via a second memory bus,

wherein, during said data transfer of said data after said data processing, said data after said data processing is transferred to said host system via said system interface and said subsequent data for said data processing is transferred from said other of said two memories to said controller via said second memory bus, and

wherein, during said data transfer of said subsequent data after said data processing, said subsequent data after said data processing is transferred to said host system via said system interface and further subsequent data for said data processing is transferred from said one of said two memories to said controller via said first memory bus.

50. (New) A storage device as claimed in Claim 46,

wherein said one of said two memories is coupled with said controller via a first memory bus, and said other of said two memories is coupled with said controller via a second memory bus,

wherein, during said data transfer of said data after said data processing, said data after said data processing is transferred to said host system via said system interface and said subsequent data for said data processing is transferred from said other of said two memories to said controller via said second memory bus, and

wherein, during said data transfer of said subsequent data after said data processing, said subsequent data after said data processing is transferred to said

host system via said system interface and further subsequent data for said data

processing is transferred from said one of said two memories to said controller via

said first memory bus.

51. (New) A storage device, comprising:

a system interface unit which carries out interface with a host system via an

external bus;

a controller coupled with said system interface which analyzes commands

received by said system interface unit from said host system and controls operations

to be performed within said storage device; and

a non-volatile semiconductor memory coupled with said controller,

wherein said non-volatile semiconductor memory is electrically erasable and

electrically programmable and stores data from said host system via said system

interface unit, and

wherein, in response to a read command received by said system interface

unit, said controller carries out overlap operations of data transferring of data after

the data processing by said controller to said host system via said system interface

unit and of data transferring of subsequent data for the data processing from said

non-volatile semiconductor memory.

52. A storage device as claimed in Claim 51, wherein said overlap operations

of said data transferring of data after the data processing to said host system via said

system interface unit and of said data transferring of subsequent data for the data

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processing from said non-volatile semiconductor memory are carried out by two memories and by said controller.

53. (New) A storage device as claimed in Claim 52, wherein, in response to said read command received by said system interface unit, one of said two memories originates said data after said data processing and another of said two memories originates said subsequent data for said data processing.

54. (New) A storage device as claimed in Claim 52, wherein said one and said other of said two memories are said non-volatile semiconductor memory.

55. (New) A storage device as claimed in Claim 54, wherein said non-volatile semiconductor memory is a flash memory.

56. (New) A storage device as claimed in Claim 53, wherein said one and said other of said two memories are said non-volatile semiconductor memory.

57. (New) A storage device as claimed in Claim 56, wherein said non-volatile semiconductor memory is a flash memory.

58. (New) A storage device as claimed in Claim 54,

wherein said one of said two memories is coupled with said controller via a first memory bus, and said other of said two memories is coupled with said controller via a second memory bus,

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wherein, during said data transfer of said data after said data processing, said data after said data processing is transferred to said host system via said system interface and said subsequent data for said data processing is transferred from said other of said two memories to said controller via said second memory bus, and

wherein, during said data transfer of said subsequent data after said data processing, said subsequent data after said data processing is transferred to said host system via said system interface and further subsequent data for said data processing is transferred from said one of said two memories to said controller via said first memory bus.

59. (New) A storage device as claimed in Claim 55,

wherein said one of said two memories is coupled with said controller via a first memory bus, and said other of said two memories is coupled with said controller via a second memory bus,

wherein, during said data transfer of said data after said data processing, said data after said data processing is transferred to said host system via said system interface and said subsequent data for said data processing is transferred from said other of said two memories to said controller via said second memory bus, and

wherein, during said data transfer of said subsequent data after said data processing, said subsequent data after said data processing is transferred to said host system via said system interface and further subsequent data for said data processing is transferred from said one of said two memories to said controller via said first memory bus.

60. (New) A storage device as claimed in Claim 56,

wherein said one of said two memories is coupled with said controller via a first memory bus, and said other of said two memories is coupled with said controller via a second memory bus,

wherein, during said data transfer of said data after said data processing, said data after said data processing is transferred to said host system via said system interface and said subsequent data for said data processing is transferred from said other of said two memories to said controller via said second memory bus, and

wherein, during said data transfer of said subsequent data after said data processing, said subsequent data after said data processing is transferred to said host system via said system interface and further subsequent data for said data processing is transferred from said one of said two memories to said controller via said first memory bus.

61. (New) A storage device as claimed in claim 57,

wherein said one of said two memories is coupled with said controller via a first memory bus, and said other of said two memories is coupled with said controller via a second memory bus,

wherein, during said data transfer of said data after said data processing, said data after said data processing is transferred to said host system via said system interface and said subsequent data for said data processing is transferred from said other of said two memories to said controller via said second memory bus, and

wherein, during said data transfer of said subsequent data after said data processing, said subsequent data after said data processing is transferred to said

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host system via said system interface and further subsequent data for said data

processing is transferred from said one of said two memories to said controller via

said first memory bus.